What is claimed is:

1. A semiconductor memory device in which a plurality of memory cells are arranged in the form of a matrix in row and column directions, the semiconductor memory device comprising:

a plurality of memory array blocks each including set numbers of memory cells, the memory array blocks being arranged in the row direction;

a Row Address Strobe (RAS) chain aligned at a first side of the plurality of memory array blocks in the row direction, the RAS chain selecting and activating a particular word line;

a Column Address Strobe (CAS) chain aligned at a second side of the plurality of memory array blocks in the column direction, the CAS chain for amplifying N bits of data from the plurality of memory array blocks and outputting the result to an input/output (IO) line, wherein N is a natural number more than 2; and

a data converter for continuously outputting the N bits of data input via the IO line from a memory array block nearest to the RAS chain to a memory array block farthest from the RAS chain.

2. The semiconductor memory device of claim 1, wherein:

the plurality of memory array blocks are arranged with respect to the RAS chain in the order of a first memory block, a second memory bock, ..., and an M^{th} memory array block, so that the first memory array block is nearest to the RAS chain and the M^{th} memory array block is farthest from the RAS chain, and

the data converter converts the N bits of data output from the first, second, ..., and the M^{th} memory array block into a first bit, a second bit, ..., an M^{th} bit of N

data pins, respectively, and outputs the result in the order from the first bit to the M^{th} bit.

3. The semiconductor memory device of claim 1, wherein the data converter may be a shift register and includes the functions of a multiplexer.

4. The semiconductor memory device of claim 1, wherein the respective memory array blocks are divided into predetermined numbers of memory sub-blocks.

5. The semiconductor memory device of claim 1, wherein the nearer a memory array block comes to the RAS chain, the greater the number of the memory sub-blocks of the memory array block.

6. The semiconductor memory device of claim 1, further comprising one repeater between every two adjacent memory array blocks,

wherein the repeater delays a control signal output from the RAS chain for a predetermined time and outputs the delayed control signal.

7. The semiconductor memory device of claim 1, wherein:

the plurality of memory array blocks further comprise a plurality of redundancy memory array blocks, and

each of the plurality of redundancy memory array blocks is arranged to have a data IO path through which data is input and output to be the same as or be faster than those to IO paths of memory array blocks, and the memory array blocks are repaired by the redundancy memory array blocks.

8. The semiconductor memory device of claim 2, wherein an output path of a first bit of the N bits of data is designed to output data faster than paths of output of data of next bits which are continuously output.

9. The semiconductor memory device of claim 4, wherein the nearer a memory array block comes to the RAS chain, the greater the number of the memory sub-blocks of the memory array block.

10. A semiconductor memory device in which a plurality of memory cells are arranged in the form of a matrix in row and column directions, the semiconductor memory device comprising:

a plurality of memory array blocks including predetermined numbers of memory cells, the memory array blocks being arranged in the row direction;

a Row Address Strobe (RAS) chain arranged at a first side of the plurality of memory array blocks in the row direction, the RAS chain for selecting and activating a particular word line;

a Column Address Strobe (CAS) chain arranged at a second side of the plurality of memory array blocks in the column direction, the CAS chain for amplifying N bits of data output from the plurality of memory array blocks and outputting the amplified N bits of data to an IO line, wherein N is a natural number more than 2; and

a plurality of multiplexers for converting the N bits of data input via the IO line into serial data and outputting the serial data,

wherein the respective memory array blocks are divided into predetermined numbers of memory sub-blocks, and

the nearer a memory array block is to the RAS chain, the smaller the number of the memory sub-blocks of the memory array block.

11. The semiconductor memory device of claim 10, wherein the respective memory array blocks substantially output N bits of data at the same point of time.